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Title:

METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

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METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE

BACKGROUND

FIELD OF THE INVENTION

[0001] The present invention relates to a method for manufacturing a semiconductor device, and, more specifically, to a method for manufacturing a semiconductor device capable of securing the stability in a polishing process for forming a landing plug.

DISCUSSTION OF RELATED ART

[0002] Generally, a polishing process is performed for an electric isolation of word lines at the time of manufacturing a semiconductor. However, after the polishing process, an insulator film is over-dished due to differences of an etching rate between the insulator film deposited for insulating of the word lines and a poly silicon film for a landing plug (hereinafter also referred to as a "LP"). Thereby, slurry residues generated during the polishing process become to remain on an upper face of the insulator film over-dished. The aforementioned slurry residues are mostly composed of metal materials having electric conductivity, and they come to remain as they are because it is difficult to remove them through the following cleaning process. The residues, as described above, affect the electric separation of word lines, seriously.

[0003] The latest technologies decrease the polishing amount on the process to

during the polishing process. However, in such a case, there are many problems in the electric separation of word lines, relatively. The reason is that the word lines of regions to be opened on forming a landing plug contact for LP are more attacked relatively than the other regions not to be opened, whereby the profile of upper word lines changes into a round shape. Therefore, the upper area of LP becomes to be larger and the electric separation margin of word lines gets more deteriorated. Though the polishing amount is increased again at the time of the polishing process to overcome these problems, the residual nitride film of word lines becomes to decrease, whereby the process of forming storage nodes and bit line self align contacts is affected and, furthermore, the short between these and tungsten silicide of word line would be generated.

SUMMARY OF THE INVENTION

[0004] The present invention is directed to a method for manufacturing a semiconductor device capable of securing the stability of a polishing process for forming a landing plug and the electric separation of word lines stably.

[0005] According to a preferred embodiment of the present invention, there is provided a method for preventing the short from taking place by improving the marginality of space when forming storage nodes or bit line self align contacts, wherein the short otherwise could be generated between storage nodes or bit line self align contacts and word lines.

[0006] One aspect of the present invention is to provide a method for manufacturing a semiconductor device comprising the steps of: preparing a

semiconductor substrate defined as an active region and a field region; forming a number of word lines in the active region and the field region of the semiconductor substrate; depositing an insulator film over the upper part of a structure to insulate word lines; patterning the insulator film to open word lines of the active region whereby forming a landing plug contact; depositing a poly silicon film to fill up the landing plug contact; performing a first polishing process using slurry including a first doping material and flattening the poly silicon film only, whereby exposing the insulator film; and forming a landing plug by performing a second polishing process using slurry including a second doping material and by flattening all the upper part of the structure.

[0007] In the aforementioned of a method for manufacturing a semiconductor device according to another embodiment of the present invention, the first doping material is preferably boron and, the concentration of said boron is preferably in the range of 2wt% to 5wt%.

[0008] In the aforementioned of a method for manufacturing a semiconductor device according to another embodiment of the present invention, the second doping material is preferably phosphorus and, the concentration of said phosphorus is preferably in the range of 2wt% to 5wt%.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Figs. 1 to 7 are cross-sectional views showing a semiconductor device for explaining a method for manufacturing a semiconductor device according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0010] Now the preferred embodiments according to the present invention will be described with reference to the accompanying drawings. Since preferred embodiments are provided for the purpose that the ordinary skilled in the art are able to understand the present invention, they may be modified in various manners and the scope of the present invention is not limited by the preferred embodiments described later.

[0011] Referring to Fig. 1, a semiconductor substrate 102 is provided, wherein the semiconductor substrate is defined as an active region and a field region and it is cleaned by the cleaning process using at least one of diluted HF (DHF), SC-1, and BOE. A field oxide film 104 is formed in the field region of the semiconductor substrate 102. The field oxide film 104 is formed to have a trench structure using shallow trench isolation (STI) process or LOCal oxidation of silicon (LOCOS) process.

[0012] Referring to Fig. 2, a number of gate electrodes 112 (hereinafter, "word lines") are formed on the semiconductor substrate 102 including the active region and the field region, which is the field oxide film 104. Word lines 112 include the gate oxide film 106, the gate layer 108, and a hard mask layer 110. The gate layer 108 includes at least one of the poly silicon films or of the doped poly silicon films, or is formed to have the structure including poly silicon films and at least one of the insulator films between poly silicon films. The hard mask layer 110 is formed with the nitride film.

[0013] Subsequently, source and drain junction areas composed of low and high-density junction areas are formed on the semiconductor substrate,

which is exposed to the both sides of word lines 112 in the active region and the field region. The low density junction area is formed by the lightly drain doped (LDD) ion-planting process. The high-density junction area is formed by the high density ion planting process using a mask as a spacer 114, wherein the spacer is formed in the both sides of word lines 112. On the other hand, the spacer 114 is formed with the nitride film thereof, or the stacked structure of the oxide film and the nitride film.

[0014] Referring to Fig. 3, the insulator film 116 is deposited over the upper part of the structure. The insulator film 116 separates word lines electrically which are formed adjacently in the active region and the field region. The insulator film 116 is formed using at least one of the group comprising spin on glass (SOG), un-doped silicate glass (USG), boron-phosphorus silicate glass (BPSG), phosphorus silicate glass (PSG), plasma enhanced tetra ethyl ortho silicate glass (PETEOS), and inter poly oxide (IPO). In addition, the insulator film 116 is deposited to fill the gap between word lines formed adjacently.

[0015] Referring to Fig. 4, a photoresist film is applied over the upper part of the structure, and then the photoresist pattern (not shown) opened locally is formed by performing exposure and development process using the photo mask, sequentially. It is preferable that the photoresist pattern is formed such that the active region is opened. In the following, the insulator film 116 is etched by the process using an etching mask as a photoresist pattern, resulting in landing plug contact (LPC) 118 formed. At this time, the etching process

for forming LPC 118 is performed by a dry etching process requiring cheaper etching cost, however, preferably a plasma dry etching process.

[0016] Referring to Fig. 5, the photoresist pattern used as the etching mask in Fig. 4 is removed through strip process. And then, the poly silicon film 120 for LP is deposited over the upper part of the structure to fill LPC 118. At this moment, it is preferable that the poly silicon film 120 for LP is deposited, thereby filling the gap between word lines formed in an LPC 118 region.

[0017] Referring to Fig. 6, the poly silicon film 120 for LP is flattened by performing a polishing process (hereinafter also referred to as "a 1st polishing process") of chemical mechanical polishing (CMP) method over the upper part of the structure. In the 1st polishing process, doping material for flattening the poly silicon film for LP 120 only is silica-based slurry with boron (B) added, for example. It is preferable that the concentration of B is in the range of 2wt% to 5wt%. In the 1st polishing process, for example, it is possible that the pressure applied to the Main brain/Retain ring/Inner tube (M/R/I) of CMP equipment is in the range of 2 to 8psi (pound/in^2), and P/H's rotation power of CMP equipment is in the range of 30 to 150rpm.

[0018] Referring to Fig. 7, a 2nd polishing process is performed over the upper part of the structure. In the above 2nd polishing process, for example, the slurry with phosphorus (P) added is used as a doping material for flattening the insulator film 116, the poly silicon film for LP 120 and the hard mask layer 110 at the same time. It is preferable that the concentration of P is in the range of 2wt% to 5wt%. In the 1st polishing process, for example, it is possible that

the pressure applied to the Main brain/Retain ring/Inner tube (M/R/I) of CMP equipment is in the range of 2 to 8psi (pound/in^2), and P/H's rotation power of CMP equipment is in the range of 30 to 150rpm. As a result, LP 122 is formed between word lines of the LPC region through the 2nd polishing process.

[0019] According to the present invention, it is possible to polish evenly and separate the adjacent word lines stably by performing the flattening process using slurry with a doping material added at the time of polishing process.

[0020] Moreover, according to the present invention, it is possible to prevent the short from taking place by securing stably the polishing process for forming a landing plug stably and improving the marginality of space when forming storage nodes or bit line self align contacts, wherein the short otherwise could be generated between the storage nodes or bit line self align contacts and word lines.

[0021] Although the foregoing description has been made with reference to the preferred embodiments, it is to be understood that changes and modifications of the present invention may be made by the ordinary skilled in the art without departing from the spirit and scope of the present invention and appended claims.